**DAILY ASSESSMENT FORMAT**

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| **Date:** | **4/06/2020** | **Name:** | **Pv sai suraksha** |
| **Course:** | **Digital Design Using HDL** | **USN:** | **4AL17EC064** |
| **Topic:** | **1.Hardware Modelling using verilog**  **2.FPGA and ASIC interview questions** | **Semester & Section:** | **6th sem**  **B section** |
| **GitHub Repository** | **surakshacourses** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**  **Hardware Modelling using Verilog:**  **\* Hardware modeling using verilog. The course will introduce the participants to the Verilog hardware description language. It will help them to learn various digital circuit modeling issues using Verilog, writing test benches, and some case studies.**    **FPGA and ASIC interview questions:**  **\* A field-programmable gate array is a semiconductor device containing programmable logic components called "logic blocks", and programmable interconnects. Logic blocks can be programmed to perform the function of basic logic gates such as AND, and XOR, or more complex combinational functions such as decoders or mathematical functions. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.**  **\*A hierarchy of programmable interconnects allows logic blocks to be interconnected as needed by the system designer, somewhat like a one-chip programmable breadboard. Logic blocks and interconnects can be programmed by the customer or designer, after the FPGA is manufactured, to implement any logical function—hence the name "field-programmable".** |

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| **Date:** | **4/06/2020** | **Name:** | **Pv sai suraksha** |
| **Course:** | **Python** | **USN:** | **4AL17EC064** |
| **Topic:** | **1.Advanced string**  **2.Advanced sets** | **Semester & Section:** | **6th sem**  **B section** |
| **AFTERNOON SESSION DETAILS** | | | |
| **Image of session**      **Advanced strings:**  **\*The '%' operator is primarily limited by the fact that it is a binary operator, and therefore can take at most two arguments. One of those arguments is already dedicated to the format string, leaving all other variables to be squeezed into the remaining argument. The current practice is to use either a dictionary or a tuple as the second argument, but as many people have commented**[**[3]**](https://www.python.org/dev/peps/pep-3101/#id9)**, this lacks flexibility. The "all or nothing" approach (meaning that one must choose between only positional arguments, or only named arguments) is felt to be overly constraining.**  **Advanced set:**  **\*Python | set() method**  **set() method is used to convert any of the iterable to sequence of iterable elements with dintinct elements, commonly called Set. Syntax : set(iterable) Parameters : Any iterable sequence like list, tuple or dictionary. Returns : An empty set if no element is passed.**  **\*Creating Python Sets**  **A set is created by placing all the items (elements) inside curly braces {} , separated by comma, or by using the built-in set() function. It can have any number of items and they may be of different types (integer, float, tuple, string etc.).** | | | |